



$$d\phi \in [2^{-6}, 2^{-\frac{26}{28}}]$$

encode:  $b_0 b_1 \dots b_{22}$

interpret:  $0000.\underbrace{00000b_0 b_1 \dots b_{22}}_{\substack{26 \text{ bit} \\ 28}}$

$$\rightarrow f \in [0.\overset{186}{\cancel{75}} \text{ Hz}, 781 \text{ kHz}]$$

$$\Delta f = \frac{75 \text{ mHz}}{186}$$

$$\phi \in [-1, 1]$$

32 ~~bits~~ wide

$b_0 b_1 b_2 b_3 . b_4 b_5 \dots b_{29}^{31}$   
 $\begin{matrix} \uparrow & \uparrow & \uparrow & \uparrow \\ 31 & 30 & 29 & 28 \end{matrix}$   $\underbrace{\hspace{1.5cm}}_{\substack{26 \text{ bit} \\ 28}}$

Signal generator output:  $\phi_{b_3}$

In every clockcycle, update phase according to:

Note:  $111.1 = -2^2 + 2^1 + 2^0 + 2^{-1} = -0.5$   
 $111.0000 = -1$

split this into conditional add on subranges, like  
 if  $b_0=0$  and  $b_3=0: \phi \pm d\phi$   
 if  $\phi[0]=1: \phi[1:] \pm d\phi[1:], \phi[0]=1$   
 to avoid shortcircuits

$\phi = \phi + d\phi$   
 if  $(b_0 == 1): b_0=0, b_1=0, b_2=0, b_3=0$  # transition negative  $\rightarrow$  positive  
 if  $(b_3 == 1 \text{ and } b_1 == 0): b_1=1, b_2=1$  # wrap around  $1 \rightarrow -1$   
 else:  $\phi \leftarrow \phi$

Note: This needs adjustments for downwards sweeping!

Input to CORDIC:  ~~$b_1 b_2 b_3 . b_4 \dots b_{23}$~~   $b_3 b_3 b_3 . b_4 \dots b_{23}$

## ddφ considerations

Issue: If ddφ is one LSB of dφ, i.e.  $2^{-28}$ , then the slowest possible ramp is  $0.186 \text{ Hz} \times 100 \text{ MHz} = 18.6 \text{ MHz/s}$ .

Solution: Instead, interpret ddφ, with a width of 23 bits, like this:

$$\phi = b_0 b_1 b_2 b_3 . b_4 b_5 b_6 b_7 b_8 b_9 \dots b_{30} b_{31}$$

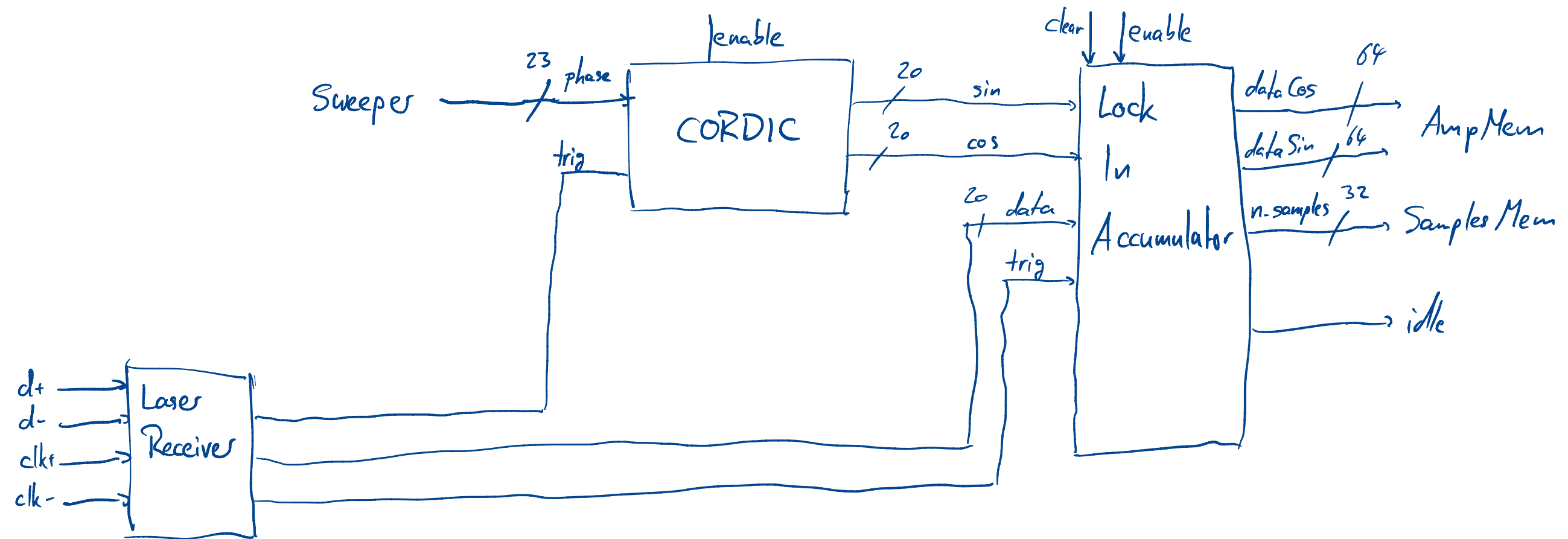
$$d\phi = 0000 . 00000 b_0 \dots b_{21} b_{22}$$

$$dd\phi = 0000 . 0000000 \dots 00 b_0 b_1 \dots b_{22}$$

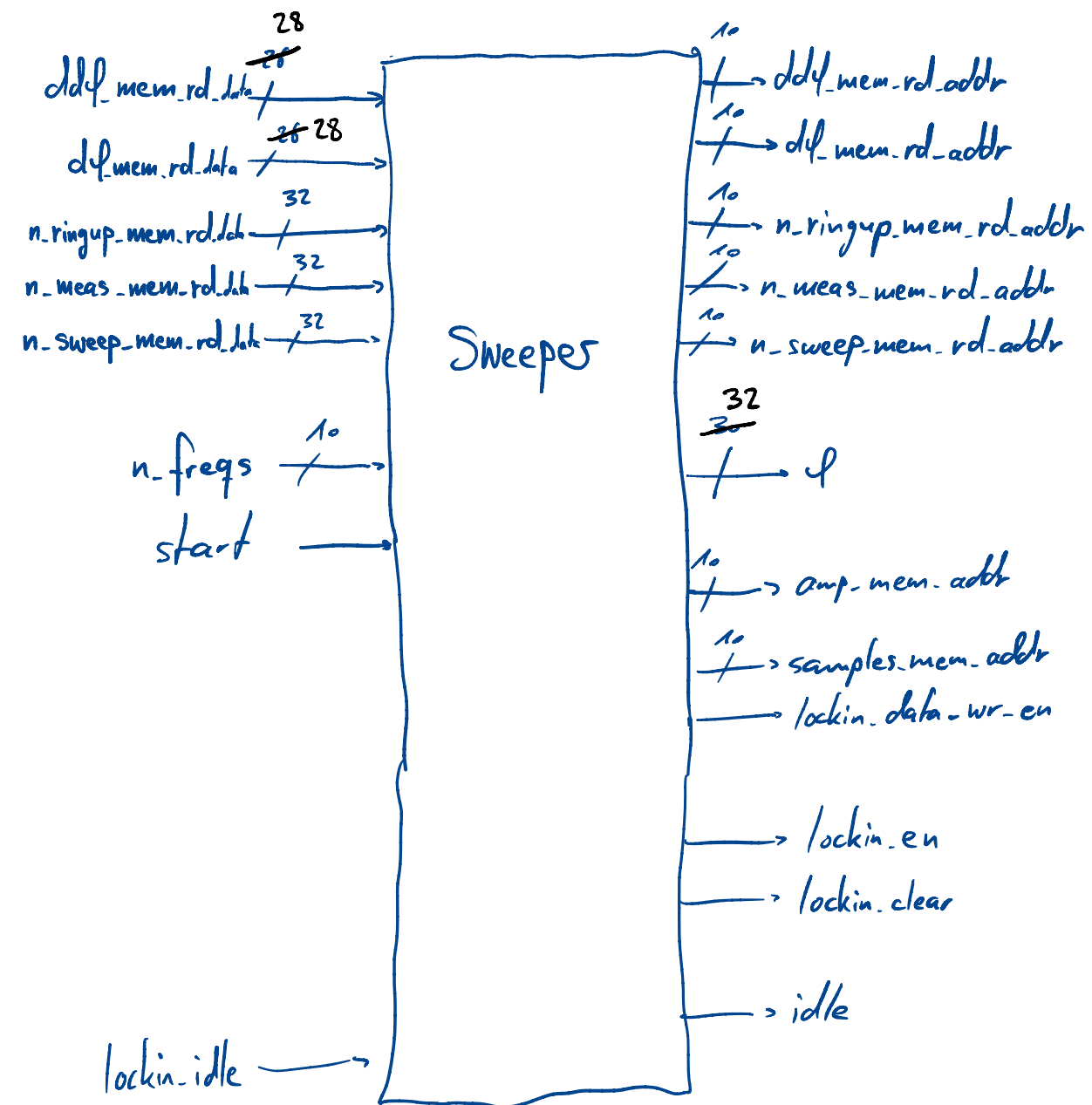
With this convention, the fastest ramp is  $\boxed{R_{\text{fast}} = 18.6 \text{ MHz} \times \frac{1}{2} \text{ Hz} = 9.3 \text{ MHz/s}}$

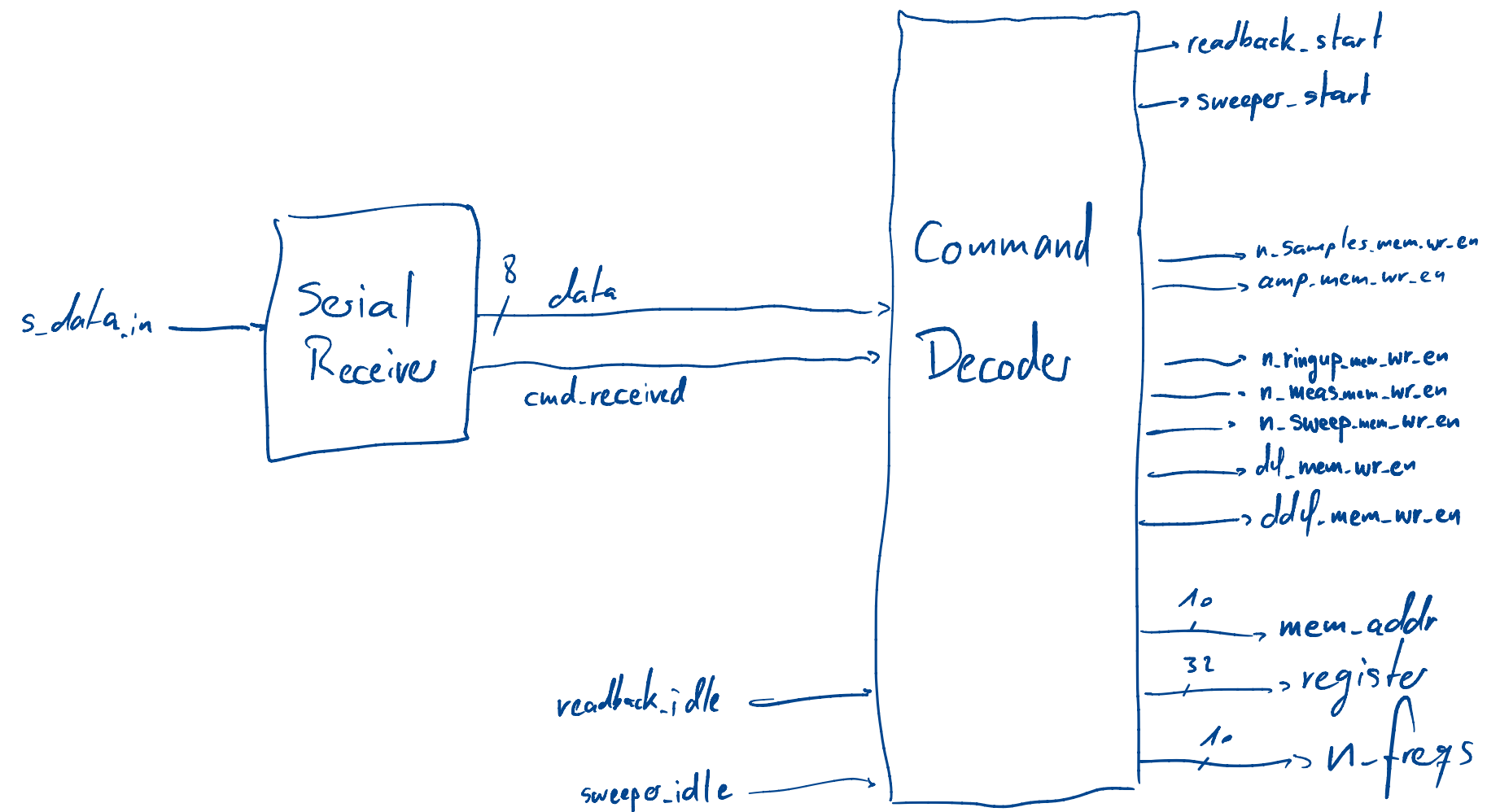
and the slowest ramp is  $\boxed{R_{\text{slow}} = 18.6 \text{ MHz} \frac{1}{2^{23}} \text{ Hz} = 2.2 \text{ Hz/s}}$

The target range is  $[10 \text{ Hz/s}, 3 \text{ MHz/s}]$ , these are guaranteed to work.  
Anything outside  $\rightarrow$  You're on your own.

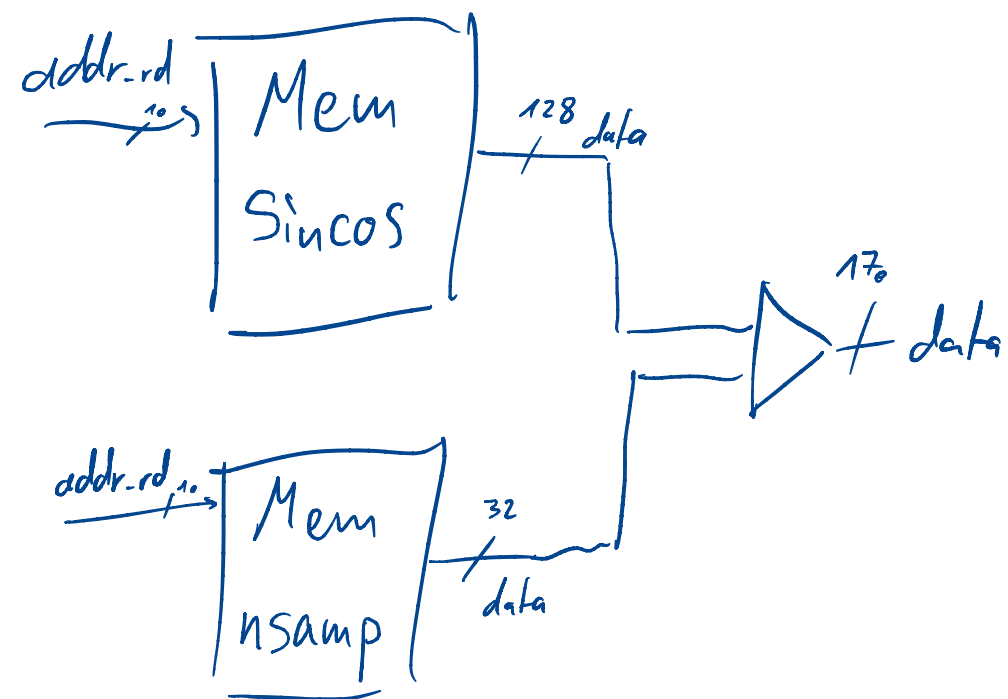
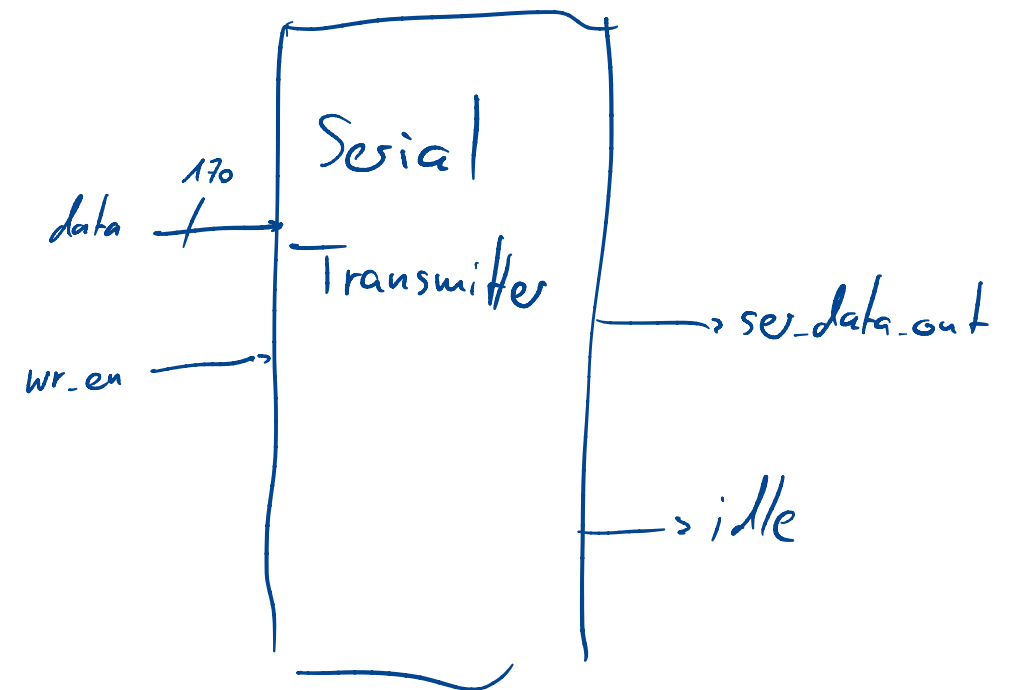
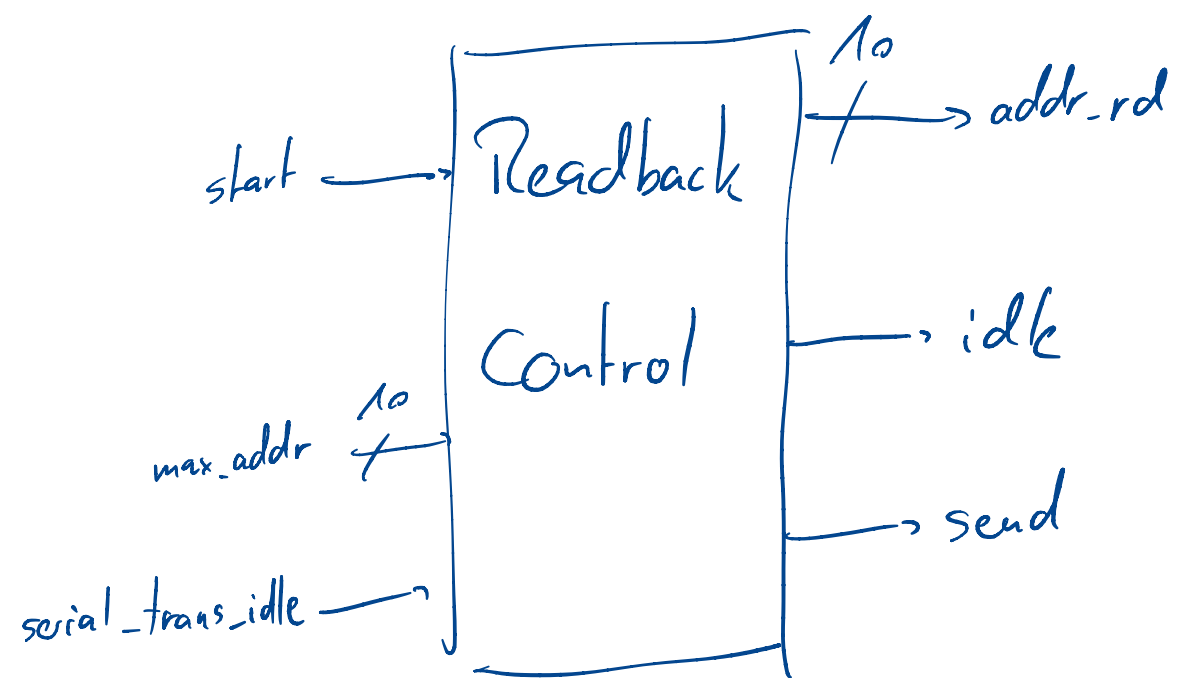




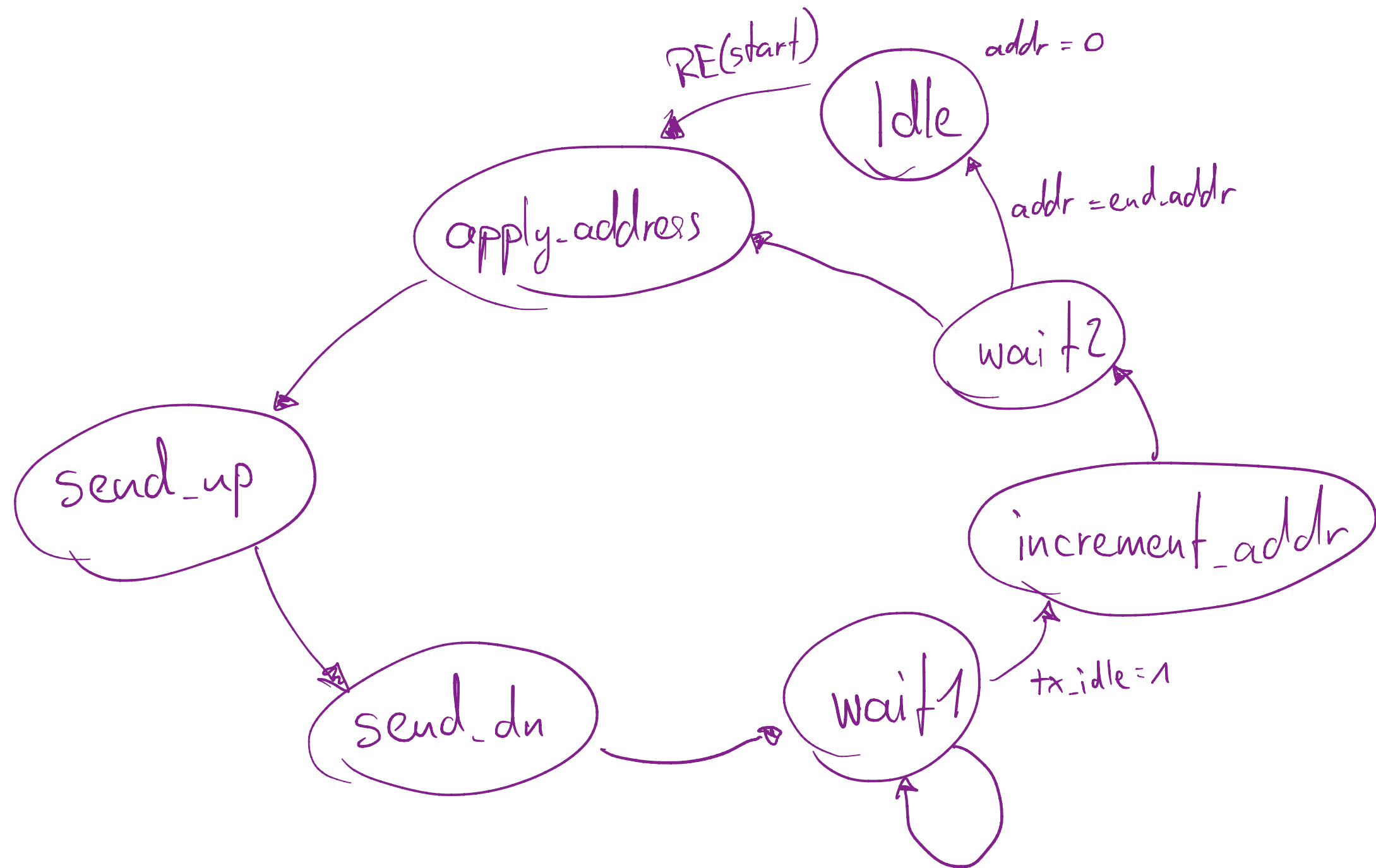




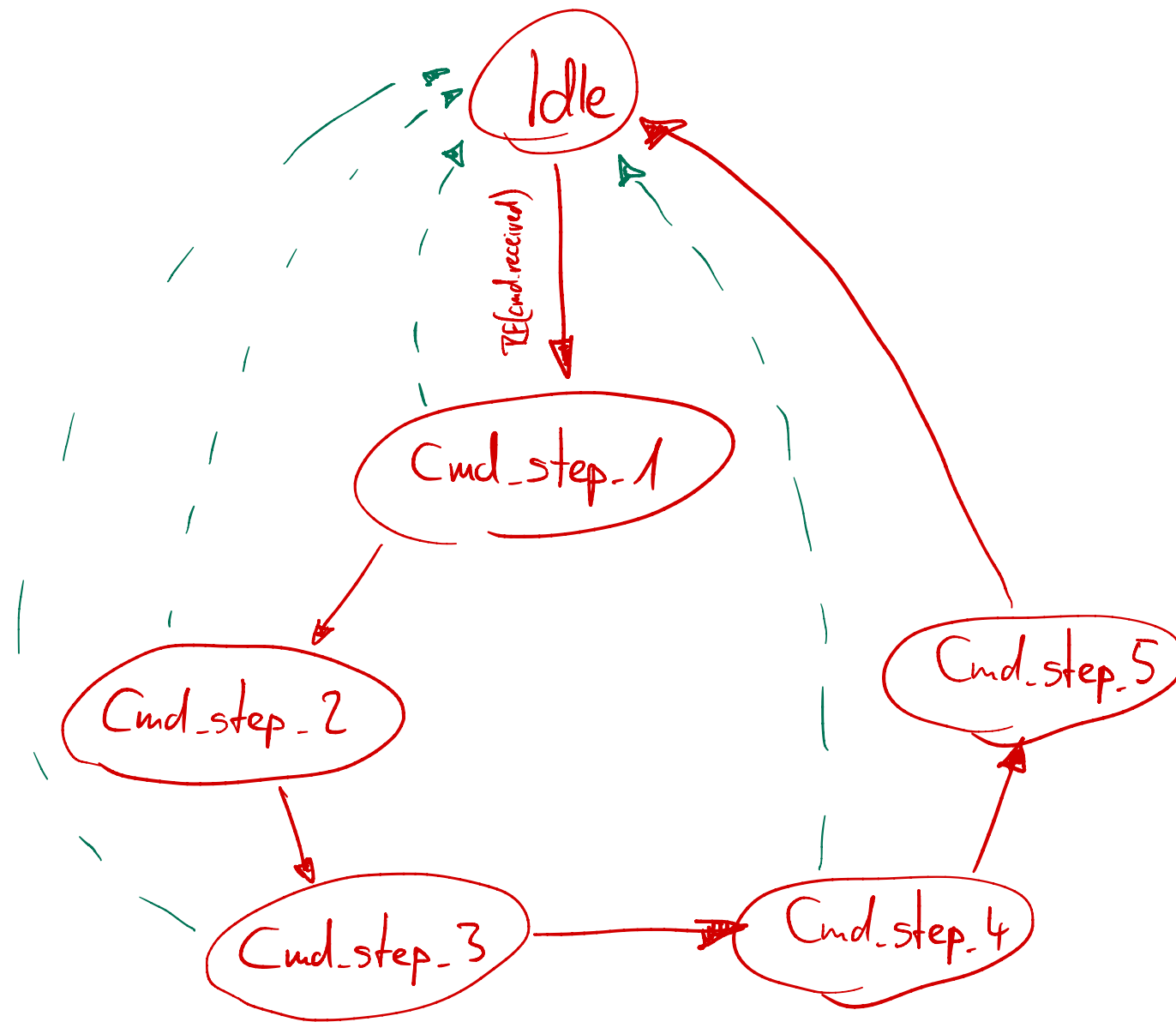
if command received and sweeper not  
idle, could trigger an LED.  
could also use LEDs to indicate various states.



# Readback Control



# Command Decoder

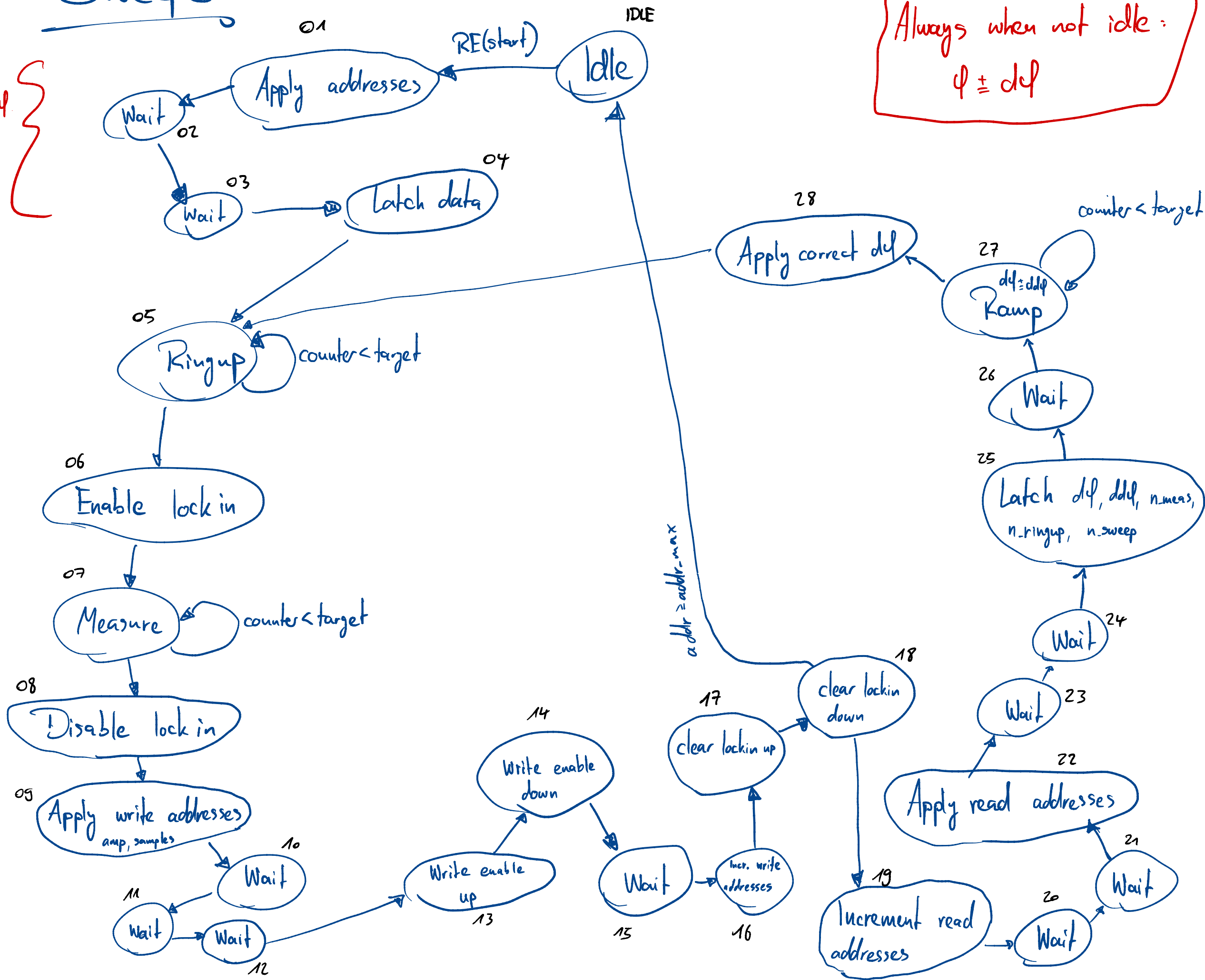


depending on opcode, early exit  
is possible

# Sweepers

Load only initial  
n.ringup, n.meas, dlf

Always when not idle:  
 $\phi \neq d\phi$



# Command Structure

destinations:

000	→	command buffer
001	→	register 4:0
010	→	register 9:5
011	→	register 14:10
100	→	register 19:15
101	→	register 24:20
110	→	register 29:25
111	→	register 61:60 → 31:30

serial packet:      b7 b6 b5      b4 b3 b2 b1 b0  
                                                                         
                         destination      payload

command payloads:

00000	move register (9:0) to address (9:0)
00001	trigger dphi write
00010	trigger nmeas write
00011	trigger nringup write
00100	trigger nsweep write
00101	trigger ddphi write
00111	move register (9:0) to nfregs (9:0)
01000	start experiment
01001	start readback
01010	reset

# ~~Read back Control FSM~~

- ~~Command Decoder FSM~~

- ~~Sweeper FSM (one process always does  $\phi \neq d\phi$ , unless idle)~~

- ~~LockIn Accumulator FSM~~

- Check if serial <sup>✓</sup> receiver and <sup>✓</sup> transmitter can easily be stoken  $\rightarrow$  Just adjust Baudrate counter targets

- Design interface/commands