

## Introduction

The Xilinx® LogiCORE™ IP Multiply Accumulator core provides implementations of multiply-accumulate using XtremeDSP™ slices. It accepts two operands, a multiplier and a multiplicand, and produces a product ( $A*B=Prod$ ) that is added/subtracted to the previous result ( $S=S+/-Prod$ ). This product value can be loaded by asserting Bypass ( $S=Prod$ ). The function can be pipelined. The Multiply Accumulator module operates on signed or unsigned data.

## Features

- Drop-in module for Virtex®-7, Virtex-6, Kintex™-7, Virtex-5, Virtex-4, Spartan®-6, Spartan-3A DSP
- Generates a multiply-accumulate function
- Supports twos complement-signed and unsigned operations
- Supports multiplier inputs ranging from 1 to 31 bits unsigned or 2 to 32 bits signed and an output width ranging from 1 to 79 bits unsigned or 2 to 80 bits signed
- Optional clock enable and synchronous clear
- Latency can be set for optimal speed or minimal pipelining
- For use with Xilinx CORE Generator™ v13.1 or later

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family <sup>(1)</sup>	Kintex-7, Virtex-7, Virtex-6, Virtex-5, Virtex-4, Spartan-6, Spartan-3A DSP/XA
Supported User Interfaces	N/A
Provided with Core	
Documentation	Product Specification
Design Files	Netlist
Example Design	Not Provided
Test Bench	No Provided
Constraints File	Not Provided
Simulation Model	Verilog/VHDL
Tested Design Tools	
Design Entry Tools	CORE Generator 13.1
Simulation	Mentor Graphics ModelSim 6.6d, Cadence Incisive Enterprise Simulator (IES) 10.2, Synopsys VCS and VCS MX 2010.06, ISIM 13.1
Synthesis Tools	N/A
Support	
Provided by Xilinx, Inc.	

1. For a complete listing of supported devices, see the [release notes](#) for this core.

## Pinout

Signal names for the core symbol are shown in [Figure 1](#) and described in [Table 1](#).

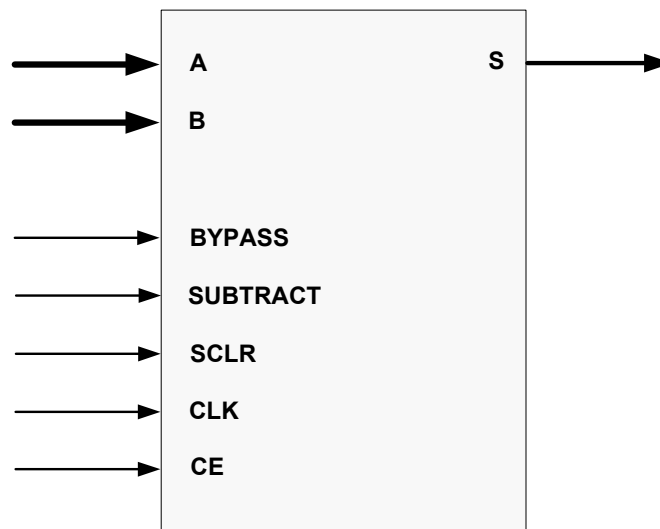


Figure 1: Core Symbol

Table 1: Core Signal Pinout

Name	Direction	Description
A[N:0]	Input	A Input bus (multiplier operand 1)
B[M:0]	Input	B Input bus (multiplier operand 2)
S[Q:0]	Output	Output bus
SUBTRACT	Input	Controls Add/Subtract operation (High = subtraction, Low = addition)
BYPASS	Input	Bypass Control Signal (Loads accumulator reg with product of A*B)
CE	Input	Clock Enable (active high)
CLK	Input	Clock signal: rising edge
SCLR	Input	Synchronous Clear (active high)

## CORE Generator Graphical User Interface Parameters

The CORE Generator GUI parameters for this module are described below:

- **Component Name:** The name of the core component to be instantiated. The name must begin with a letter and be composed of the following characters: a to z, 0 to 9, and “\_”.
- **A Input Width:** Sets the width of the Port A (multiplier operand 1) input. The valid range is 1 to 31 unsigned and 2 to 32 signed. The default value is 16.
- **B Input Width:** Sets the width of the Port B (multiplier operand 2) input. The valid range is 1 to 31 unsigned and 2 to 32 signed. The default value is 16.
- **A Input Type:** Sets the type of the Port A data: Signed, Unsigned. The default value is Signed.
- **B Input Type:** Sets the type of the Port B data. Signed, Unsigned. The default value is Signed.
- **Accumulation Width:** Sets the internal width of the accumulation function. The valid range is **A Input Width** + **B Input Width** + the number of "unsigned" inputs (0, 1, or 2) to 80. The default value is 48.
- **Output Width:** Sets the output width. The valid range is 2 to **Accumulation Width**. The default value is 16.
- **Accumulation Mode:** Sets the mode of operation of the module. Valid values are Add, Subtract, and Add-Subtract. If an adder/subtractor is specified, the SUBTRACT pin sets the mode of operation. The default is Add.
- **Bypass:** When set to true, creates a BYPASS pin. Activating the BYPASS pin sets the output to be the value given by the product of A and B. The default is for no BYPASS pin to be generated. The default value is false.
- **Bypass Sense:** Set to Active High or Active Low. The default value is Active High.
- **Synchronous Controls and Clock Enable (CE) Priority:** This parameter controls whether or not the SCLR input is qualified by CE. When set to “Sync Overrides CE”, SCLR overrides the CE signal. When set to “CE Overrides Sync”, SCLR has an effect only when CE is high. The default is “Sync Overrides CE”.
- **Latency Configuration:** Automatic or Manual; Automatic sets optimal latency for maximum speed; Manual sets **Latency** to 1 or the *optimal value*. The default is Manual.
- **Latency:** Value used for latency when **Latency Configuration** is set to Manual: Two possible values are "1" (minimal latency) and "*optimal latency*". See the section, [Pipelined Operation](#) for more information. The default value is 1.

Table 2 is a cross-reference table from the GUI parameters listed above to the XCO parameter names in the XCO file. The ranges and default values are also shown to facilitate data retrieval from the text above.

Table 2: CORE Generator GUI and XCO Parameters

GUI Name	Default Value	Valid Range	XCO Parameter
Component Name	MultAccum	..	Component_Name
A Input Width	16	1..31 unsigned 2..32 signed	A_Input_Width
A Input Type	Signed	Signed, Unsigned	A_Input_Type
B Input Width	16	1..31 unsigned 2..32 signed	B_Input_Width
B Input Type	Signed	Signed, Unsigned	B_Input_Type
Accumulation Width	48	<b>A Input Width + B Input Width</b> + number of unsigned inputs (0, 1, or 2)..80	Accum_Width
Output Width	16	2.. <b>Accumulation Width</b>	Output_Width
Accumulation Mode	Add	Add, Subtract, Add_Subtract	Accum_Mode
Bypass	true	true, false	Bypass
Bypass Sense	Active_High	Active_Low, Active_High	Bypass_Sense
Latency Configuration	Manual	Automatic, Manual	Latency_Configuration
Latency	1 (minimum latency)	1	Latency
Synchronous Controls and Clock Enable (CE) Priority	Sync_Overrides_CE	Sync_Overrides_CE, CE_Overrides_Sync	Sync_CE_Priority

## Core Use through CORE Generator

The CORE Generator GUI performs error-checking on all input parameters. Resource estimation and latency information are also available.

Several files are produced when a core is generated, and customized instantiation templates for Verilog and VHDL design flows are provided in the .veo and .vho files, respectively. For detailed instructions, see the CORE Generator software documentation.

## Simulation Models

The core has a number of options for simulation models:

- VHDL behavioral model in the xilinxcorelib library
- VHDL UniSim structural model
- Verilog UniSim structural model

Xilinx recommends that simulations utilizing UniSim-based structural models are run using a resolution of 1 ps. Some Xilinx library components require a 1 ps resolution to work properly in either functional or timing simulation. The UniSim-based structural models might produce incorrect results if simulation with a resolution other than 1 ps. See the “Register Transfer Level (RTL) Simulation Using Xilinx Libraries” section in *Synthesis and Simulation Design Guide* for more information. This document is part of the ISE® Software Manuals set available at:

[www.xilinx.com/support/software\\_manuals.htm](http://www.xilinx.com/support/software_manuals.htm)

## Pipelined Operation

The Multiply Accumulator module can be optionally pipelined to meet two conditions:

- to provide the *minimal* amount of latency allowed by the function. Achieved by setting:
  - **Latency Configuration** = Manual and **Latency** = 1
- to provide the *optimal* amount of latency allowed. This can be achieved in two ways:
  - **Latency Configuration** = Automatic or
  - **Latency Configuration** = Manual and **Latency** = *optimal value*

For minimal latency (Latency = 1), only accumulation registers will be present.

If bypass is requested on a pipelined module, the bypass value will appear on the outputs after the number of clock cycles, specified by the latency control.

## Performance and Resource Utilization

Table 3 and Table 4 provide Multiply Accumulator performance and resource usage for a number of different configurations.

The maximum clock frequency results were obtained by double-registering input and output ports to reduce dependence on I/O placement. The inner level of registers used a separate clock signal to measure the path from the input registers to the first output register through the core.

The resource usage results do not include the above "characterization wrapper" registers and represent the true logic used by the core.

The map options used were: “map -pr b -ol high.”

The par options used were: “par -ol high.”

Clock frequency does not take clock jitter into account and should be derated by an amount appropriate to the clock source jitter specification.

The maximum achievable clock frequency and the resource counts may also be affected by other tool options, additional logic in the FPGA device, using a different version of Xilinx tools, and other factors. The Xilinx SmartXplorer™ script can be used to find the optimal settings.

All characterization was performed using the following parameter settings unless otherwise noted:

- **A Input Type** = Signed
- **B Input Type** = Signed
- **Synchronous Controls and Clock Enable(CE) Priority** = Sync\_Overrides\_CE
- **Accumulation Width** = Output Width

**Table 3: XtremeDSP Slice Multiply Accumulator: Virtex-5 (Part = XC5VSX50T-1)**

Description	Optimal Pipelining				
A Input Width	16	30	26	16	30
B Input Width	16	10	20	16	30
Output Width	45	45	47	64	64
Latency: (actual)	3	6	6	4	8
Max Clock Frequency (MHz)	444	444	444	444	367
LUT6-FF pairs	0	17	17	48	257
LUT6s	0	0	0	0	69
Flip-flops	0	17	17	48	256
DSP48Es	1	3	3	2	4

**Table 4: XtremeDSP Slice Multiply Accumulator: Spartan-3A DSP (Part = XC3SD3400A-4)**

Description	Optimal Pipelining				
A Input Width	16	20	20	16	26
B Input Width	16	16	22	16	24
Output Width	45	45	46	54	54
Latency: (actual)	3	7	10	5	10
Max Clock Frequency (MHz)	250	250	250	174	167
LUT6s	0	3	47	56	137
Flip-flops	0	42	168	88	286
DSP48As	1	3	5	1	4

## Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

See the IP Release Notes Guide ([XTP025](#)) for further information on this core.

For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

## Ordering Information

This LogiCORE IP module is included at no additional cost with the Xilinx ISE Design Suite development software and is provided under the terms of the Xilinx End User License Agreement. To generate the core, use the Xilinx CORE Generator system v13.1, which is included with the ISE Design Suite.

For more information, visit the [core](#) page.

Please contact your local Xilinx [sales representative](#) for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx [IP Center](#).

## Revision History

Date	Version	Description of Revisions
4/24/2009	2.0	First customer release of Multiply Accumulator core.
3/01/2011	2.1	Added support for Virtex-7 and Kintex-7.

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